REMARKS

Applicant respectfully requests reconsideration of this application in view of the following remarks. For the Examiner's convenience and reference, Applicant's remarks are presented in substantially the same order in which the corresponding issues were raised in the Office Action.

Status of the Claims

Claims 1-20 are pending. Claims 1, and 8 are currently amended to more clearly define pre-existing claim limitations. No claims are canceled. No claims are added. No new matter has been added.

Summary of the Office Action

Claims 1-7 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,356,106 to Greeff et al. (hereinafter "Greef ('106)").

Claims 8-11, 13, and 15-17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,871,253 to Greeff et al. (hereinafter "Greef ('253)").

Claims 12, 14, and 18-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Greeff ('253) in view of U.S. Patent No. 6,308,232 to Gasbarro (hereinafter "Gasbarro").

Response to Rejections under 35 U.S.C. § 102(b)

The Office Action rejected claims 1-7 under 35 U.S.C. § 102(b) as being anticipated by Greeff ('106). Applicant respectfully requests withdrawal of these rejections because the cited reference fails to disclose all of the limitations of the claims.

CLAIMS 1-7

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Greeff ('106). Applicant respectfully submits that claim 1 is patentable over the cited reference because Greeff ('106) does not disclose all of the limitations of the claim. Claim 1, as amended, recites:

> A memory device, comprising:
> an address bus interface;

an address bus termination circuit that can be enabled or disabled; and

an address bus termination control signal input, **wherein the address bus termination control signal input is operable to enable the address bus termination circuit when the address bus termination control signal input is tied to a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit when the address bus termination control signal input is tied to a second voltage level.** (Emphasis added).

In support of the rejection, the Office Action states, in part:

> With regard to claim 1, Greeff et al. describe a memory device comprising:
>
> An address bus interface (column 3, lines 34 -40; Figure 1, item 102);
>
> An address bus termination circuit that can be enabled or disabled (Figure 1, item 120; column 4, lines 21 -31);
>
> An address bus termination signal input (Figure 1, TERMINATION ENABLE; column 4, lines 21 -46);
>
> With regard to claim .2, Greeff et al. implicitly describe the address bus termination circuit to be enabled if an asserted address bus termination control signal is received at the address bus termination control signal input since they describe **driving the control signal input to where the termination circuit is enabled** (column 4, lines 21 - 31). Examiner identifies this as being equivalent to asserting the control signal. Office Action, November 9, 2005, pp. 2-4 (emphasis added).

Applicant respectfully disagrees with the Office Action's characterization of the prior art because Greeff ('106) fails to disclose all of the limitations of the claim. In particular, Greeff ('106) does not disclose an address bus termination control signal input, wherein the address bus termination control signal input is operable to enable the address bus termination circuit when the address bus termination control signal input is tied to a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit when the address bus termination control signal input is tied to a second voltage level.

Greeff ('106) is directed to an active termination circuit incorporated into the devices connected to a multidrop bus. Greeff ('106), Abstract. "[T]he active termination circuit 120 includes a switch 122 connected between a 'trimmable' termination resistor

124, having a trimmable termination resistance RTERM, and a reference voltage VTERM. It is desirable that the termination circuit 120 comprises a simple termination network that can be switched on and off very quickly." See Greeff ('106) col. 3, lines 65 to col. 4, lines 1-5. "The active termination circuit 120 can be programmed into one of two states. ... The active termination circuit 120 can be programmed into the termination enabled state by driving the termination enable signal TERMINATION ENABLE to a level that will close the switch 122. ... The active termination circuit 120 can be programmed into the termination disabled state by driving the termination enable signal TERMINATION ENABLE to a level that will open the switch 122. See col. 4, lines 20-46. In operation, termination can be enabled in some devices 110 and disabled in other devices 110 depending upon the communication traffic on the bus 102. See col. 5, lines 1-3. Driving the TERMINATION ENABLE to a level that will open the switch based upon the communication traffic on the bus 102 does not constitute an address bus termination control signal input, wherein the address bus termination control signal input is operable to enable the address bus termination circuit when the address bus termination control signal input is tied to a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit when the address bus termination control signal input is tied to a second voltage level, because the TERMINATION ENABLE is driven by signals on the bus.

In contrast, claim 1 recites "an address bus termination control signal input, **wherein the address bus termination control signal input is operable to enable the address bus termination circuit when the address bus termination control signal input is tied to a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit when the address bus termination control signal input is tied to a second voltage level.**" For the reasons stated above, Greeff ('106) fails to disclose all of the limitations of claim 1. In particular, Greeff ('106) does not disclose an address bus termination control signal

input, wherein the address bus termination control signal input is operable to enable the address bus termination circuit when the address bus termination control signal input is tied to a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit when the address bus termination control signal input is tied to a second voltage level. Given that the cited reference fails to disclose all of the limitations of the claim, Applicant respectfully submits that claim 1 is patentable over the cited reference. Accordingly, Applicant requests that the rejection of claim 1 under 35 U.S.C. § 102(b) be withdrawn.

Given that claims 2-7 depend from independent claim 1, which is patentable over the cited reference, Applicant respectfully submits that dependent claims 2-7 are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of claims 2-7 under 35 U.S.C. § 102(b).

The Office Action rejected claims 8-11, 13, and 15-17 under 35 U.S.C. § 102(b) as being anticipated by Greeff ('253). Applicant respectfully requests withdrawal of these rejections because the cited reference fails to disclose all of the limitations of the claims.

CLAIMS 8-11, 13, 15, AND 16

Claim 8 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Greeff ('253). Applicant respectfully submits that claim 8 is patentable over the cited reference because Greeff ('253) does not disclose all of the limitations of the claim. Claim 8 recites:

> A memory module, comprising:
>
> a plurality of memory devices coupled to an address bus in a daisy chain configuration, each of the plurality of memory devices including
>
> an address bus interface,
>
> an address bus termination circuit that can be enabled or disabled, and
>
> an address bus termination control signal input, **wherein the address bus termination control signal input is operable to enable the address bus termination circuit when the address bus termination control signal input is tied to a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit**

when the address bus termination control signal input is tied to a second voltage level. (Emphasis added).

In support of the rejection, the Office Action states, in part:

> With regard to claim 8, Greeff et al. describe a memory module comprising:
>
> A plurality of memory devices coupled to an address bus in a daisy chain configuration, each of the plurality of memory devices including:
>
> An address bus interface (Figure 14, item 28; column 4, lines 1 -6, 25 -27);
>
> An address bus termination circuit that can be enabled or disabled (Figure 14, item 302; further described in column 9, line 59 -column 1O, line 3; column 11, lines 46 -52);
>
> **An address bus termination control signal input (column 9, lines 12 -24; where a control signal input may be interpreted as a selection signal input).** Office Action, November 9, 2005, pp. 8-10 (emphasis added).

Applicant respectfully disagrees with the Office Action's characterization of the prior art because Greeff ('253) fails to disclose all of the limitations of the claim. In particular, Greeff ('253) does not disclose an address bus termination control signal input, wherein the address bus termination control signal input is operable to enable the address bus termination circuit when the address bus termination control signal input is tied to a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit when the address bus termination control signal input is tied to a second voltage level.

Greeff ('253) is directed to a method and associated apparatus for improving the performance of a high speed memory bus using switches. Greeff ('253), Abstract. The selection signal input, as referred to by the Examiner, does not constitute an address bus termination control signal because the selection signal controls the two-way switches 302, which are used to "to connect [or disconnect] the memory controller 31 to the first memory module 24 in a point-to-point data connection," and does not control the terminating resisters 38 or terminators 452. See Greeff ('235), col. 9, lines 9-34, and Abstract.

Morevover, Greef ('253) discloses that "[t]he bus terminating resistors 38 may be switched terminators to permit switchable termination (i.e., termination enabled (ON) or termination disabled (OFF)) for varying data transfer operations." See col. 11, lines 46-

48. Greeff ('253) also discloses "programmable active termination," as described in Greeff ('106).

Greeff ('106) is directed to an active termination circuit incorporated into the devices connected to a multidrop bus. Greeff ('106), Abstract. "[T]he active termination circuit 120 includes a switch 122 connected between a 'trimmable' termination resistor 124, having a trimmable termination resistance RTERM, and a reference voltage VTERM. It is desirable that the termination circuit 120 comprises a simple termination network that can be switched on and off very quickly." See Greeff ('106) col. 3, lines 65 to col. 4, lines 1-5. "The active termination circuit 120 can be programmed into one of two states. ... The active termination circuit 120 can be programmed into the termination enabled state by driving the termination enable signal TERMINATION ENABLE to a level that will close the switch 122. ... The active termination circuit 120 can be programmed into the termination disabled state by driving the termination enable signal TERMINATION ENABLE to a level that will open the switch 122. See col. 4, lines 20-46. In operation, termination can be enabled in some devices 110 and disabled in other devices 110 depending upon the communication traffic on the bus 102. See col. 5, lines 1-3. Driving the TERMINATION ENABLE to a level that will open the switch based upon the communication traffic on the bus 102 **does not constitute** wherein the address bus termination control signal input is operable to enable the address bus termination circuit when the address bus termination control signal input is tied to a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit when the address bus termination control signal input is tied to a second voltage level because the TERMINATION ENABLE is driven by signals on the bus.

In sum, the selection signal controls the switches 302, and not the switch of the switchable resister 28. In addition, programmable active termination, as described in Greeff '106 does not constitute an address bus termination control signal input, wherein the address bus termination control signal input is operable to enable the address bus termination circuit when the address bus termination control signal input is tied to a first voltage level, and wherein the address bus termination control signal input is operable to

disable the address bus termination circuit when the address bus termination control signal input is tied to a second voltage level.

In contrast, claim 8 recites "an address bus termination control signal input, **wherein the address bus termination control signal input is operable to enable the address bus termination circuit when the address bus termination control signal input is tied to a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit when the address bus termination control signal input is tied to a second voltage level.**" For the reasons stated above, Greeff ('253) fails to disclose all of the limitations of claim 8. In particular, Greeff ('253) does not disclose an address bus termination control signal input, wherein the address bus termination control signal input is operable to enable the address bus termination circuit when the address bus termination control signal input is tied to a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit when the address bus termination control signal input is tied to a second voltage level. Given that the cited reference fails to disclose all of the limitations of the claim, Applicant respectfully submits that claim 8 is patentable over the cited reference. Accordingly, Applicant requests that the rejection of claim 8 under 35 U.S.C. § 102(b) be withdrawn.

Given that claims 9-11, 13, 15, and 16 depend from independent claim 8, which is patentable over the cited reference, Applicant respectfully submits that dependent claims 9-11, 13, 15, and 16 are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of claims 9-11, 13, 15, and 16 under 35 U.S.C. § 102(b) and the rejection of claims 12 and 14 under 35 U.S.C. § 103(a) be withdrawn.

CLAIM 17

Claim 17 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Greeff ('253). Applicant respectfully submits that claim 17 is patentable over the cited reference because Greeff ('253) does not disclose all of the limitations of the claim. Claim 17, as amended, recites:

> A method, comprising:
>
> connecting in a daisy chain configuration an address bus to a plurality of memory devices on a memory module;

providing address bus termination circuitry in the plurality of memory devices; and

enabling the address bus termination circuitry of only one of the plurality of memory devices. (Emphasis added).

In support of the rejection, the Office Action states, in part:

> With regard to claim 17, Greeff et al. describe a method comprising:
>
> Connecting in a daisy chain configuration an address bus to a plurality of memory devices on a memory module (Figure 14, item 28; column 4, lines 1 -6, 25 - 27);
>
> Providing address bus termination circuitry in the plurality of memory devices (Figure 14, item 302; further described in column 11, lines 46 -52);
>
> Enabling the address bus termination circuitry of only one of the plurality of memory devices. Greeff et al. provide no reason as to why their invention would not be capable of enabling the termination circuitry for only a single memory device, and therefore describe this limitation (Figure 14, item 302; column 9, line 59 -column 10, line 3; column 11, lines 46 -52). Office Action, November 9, 2005, pp. 10-11 (emphasis added).

Applicant respectfully disagrees with the Office Action's characterization of the prior art because Greeff ('253) fails to disclose all of the limitations of the claim. In particular, Greeff ('253) does not disclose enabling the address bus termination circuitry of only one of the plurality of memory devices.

Greeff ('253) is directed to a method and associated apparatus for improving the performance of a high speed memory bus using switches. Greeff ('253), Abstract. The selection signal input, as referred to by the Examiner, does not constitute an address bus termination control signal because the selection signal controls the two-way switches 302, which are used to "to connect [or disconnect] the memory controller 31 to the first memory module 24 in a point-to-point data connection," and does not control the terminating resisters 38 or terminators 452. See Greeff ('235), col. 9, lines 9-34, and Abstract. Greeff ('253) does not disclose enabling the address bus termination circuitry of only one of the plurality of memory devices.

In contrast, claim 17 recites "enabling the address bus termination circuitry of only one of the plurality of memory devices." For the reasons stated above, Greeff ('253) fails to disclose all of the limitations of claim 17. In particular, Greeff ('253) does not

disclose enabling the address bus termination circuitry of only one of the plurality of memory devices. Given that the cited reference fails to disclose all of the limitations of the claim, Applicant respectfully submits that claim 17 is patentable over the cited reference. Accordingly, Applicant requests that the rejection of claim 17 under 35 U.S.C. § 102(b) be withdrawn.

Given that claims 18-20 depend from independent claim 17, which is patentable over the cited reference, Applicant respectfully submits that dependent claims 18-20 are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of claims 18-20 under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

It is respectfully submitted that in view of the amendments and remarks set forth herein, the rejections and objections have been overcome. If the Examiner believes a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Thomas Ferrill at (408) 720-8300.

If there are any additional charges, please charge them to Deposit Account No. 02-2666.

Respectfully submitted,

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